AMENDMENTS TO THE CLAIMS

1. (Currently amended) A circuit for sampling and holding, comprising:

a processing circuit that is interleaved such that the processing circuit comprises a first processing channel and a second processing channel;

a first sample-and-hold channel, comprising:

a first sampling switch circuit that is coupled between a first node and a second node;

a first sampling capacitor circuit that is coupled to the second node; and

a first holding switch circuit that is coupled between the second node and the first processing channel; and

a second sample-and-hold channel, comprising:

a second sampling switch circuit that is coupled between the first node and a third node;

a second sampling capacitor circuit that is coupled to the third node; and

a second holding switch circuit that is coupled between the third node and the second processing channel, wherein the first sampling switch circuit is configured to be closed during a sample phase for the first sample-and-hold channel, and wherein the first hold switch circuit is configured to be open during the sample phase for the first sample-and-hold channel.

2. (Original) The circuit of Claim 1, further comprising a buffer circuit having an output that is coupled to the first node.

3. (Original) The circuit of Claim 1, wherein the first sample-and-hold channel further comprises a buffer circuit that is coupled between the first sampling switch and the first holding switch circuit, and wherein the second sample-and-hold channel further comprises another buffer circuit that is coupled between the second sampling switch and the second holding switch circuit.

4. (Currently amended) A circuit for sampling and holding, comprising:

a processing circuit that is interleaved such that the processing circuit comprises a first processing channel and a second processing channel;

a first sample-and-hold channel, comprising:

a first sampling switch circuit that is coupled between a first node and a second node;

a first sampling capacitor circuit that is coupled to the second node; and

a first holding switch circuit that is coupled between the second node and the first processing channel; and

a second sample-and-hold channel, comprising:

a second sampling switch circuit that is coupled between the first node and a third node;

a second sampling capacitor circuit that is coupled to the third node; and

a second holding switch circuit that is coupled between the third node and the second processing channel~~The circuit of Claim 1~~, wherein the processing circuit includes an interleaved analog-to-digital conversion circuit, the first processing channel includes a first bank of the interleaved analog-to-digital conversion circuit, and the second processing channel includes a second bank of the interleaved analog-to-digital conversion circuit.

5. (Currently amended) A circuit for sampling and holding, comprising:

a processing circuit that is interleaved such that the processing circuit comprises a first processing channel and a second processing channel;

a first sample-and-hold channel, comprising:

a first sampling switch circuit that is coupled between a first node and a second node;

a first sampling capacitor circuit that is coupled to the second node; and

a first holding switch circuit that is coupled between the second node and the first processing channel; and

a second sample-and-hold channel, comprising:

a second sampling switch circuit that is coupled between the first node and a third node;

a second sampling capacitor circuit that is coupled to the third node; and

a second holding switch circuit that is coupled between the third node and the second processing channel; and~~The circuit of Claim 1, further comprising:~~

a boost circuit that is configured to provide a boosted signal from a clock signal such that the boosted signal substantially corresponds to a boosted voltage during a hold phase, wherein the clock signal is configured to alternate between a first voltage level and a second voltage level, the second voltage level corresponds to a high power supply voltage, and wherein the boosted voltage exceeds the high power supply voltage.

6. (Original) The circuit of Claim 5, wherein the first and second holding switch circuits each include:

a first boosted switch circuit that is configured to open and close in response to the boosted signal; and

a first dummy circuit that is configured to absorb channel charge from the boosted switch circuit if the boosted switch circuit closes.

7. (Currently amended) The circuit of Claim 1, wherein:

the first sampling switch circuit is ~~configured to be closed during a sample phase for the first sample-and-hold channel, and~~ further configured to be open during a hold phase for the first sample-and-hold channel;

the first hold switch circuit is ~~configured to be open during the sample phase for the first sample-and-hold channel, and~~ further configured to be closed during the hold phase for the first sample-and-hold channel;

the second sampling switch circuit is configured to be closed during a sample phase for the second sample-and-hold channel, and further configured to be open during a hold phase for the second sample-and-hold channel; and wherein

the second hold switch circuit is configured to be open during the sample phase for the second sample-and-hold channel, and further configured to be closed during the hold phase for the second sample-and-hold channel.

8. (Original) The circuit of Claim 7, wherein the sample phase for the first sample-and-hold channel takes half of a period of a sampling control signal and occurs once per period of the sampling control signal, and wherein the first sample-and-hold channel is arranged such that the first processing channel has an amount of time substantially equal to one full period of the sampling control signal to process a signal received from the first holding switch circuit.

9. (Original) The circuit of Claim 7, wherein the sample phase for the first sample-and-hold channel occurs at substantially the same time as the hold phase for the second sample-and-hold channel, and wherein the hold phase for the first sample-and-hold channel occurs at substantially the same time as the sample phase for the second sample-and-hold channel.

10. (Original) A circuit for sampling and holding, comprising:

a first sampling switch circuit that is coupled between a first node and a second node;

a sampling capacitor circuit that is coupled to the second node;

a holding switch circuit that is coupled between the second node and a third node, wherein the holding switch comprises:

a first boosted switch circuit that is configured to open and close in response to a boosted signal; and

a first dummy circuit that is configured to absorb channel charge from the boosted switch circuit if the boosted switch circuit closes; and

a boost circuit that is configured to provide the boosted signal from a clock signal such that the boosted signal substantially corresponds to a boosted voltage during a hold phase, and such that the boosted voltage exceeds a high power supply voltage, wherein the clock signal is configured to alternate between a first voltage level and a second voltage level, and wherein the second voltage level corresponds to the high power supply voltage.

11. (Original) The circuit of Claim 10, wherein the boosted signal corresponds to an off voltage during a sample phase, the off voltage is significantly greater than a low power supply voltage, and wherein the first voltage level corresponds to the low power supply voltage.

12. (Original) The circuit of Claim 10, wherein the holding switch circuit further includes a second dummy circuit.

13. (Original) The circuit of Claim 12, wherein the first dummy circuit includes a first n-type transistor including a drain that is coupled to a source of the first n-type transistor, the second dummy circuit includes a second n-type transistor including a drain that is coupled to a source of the second n-type transistor, and wherein the first boosted switch circuit includes a third n-type transistor.

14. (Original) The circuit of Claim 12, wherein the first dummy circuit is configured to receive an inverted boosted signal, the second dummy circuit is configured to receive another inverted boosted signal, and wherein the inverted boosted signal and the other inverted boosted signal are each a substantial inverse of the boosted signal.

15. (Original) The circuit of Claim 12, wherein the first and second dummy circuits each include an associated width that is approximately half of a width that is associated with the first boosted switch circuit.

16. (Original) The circuit of Claim 12, wherein the first dummy circuit is coupled between the second node and the first boosted switch circuit, and wherein the second dummy circuit is coupled between the first boosted switch circuit and the third node.

17. (Original) The circuit of Claim 12, wherein the holding switch circuit further includes:

a second boosted switch circuit that is configured to open and close in response to another boosted signal, wherein the other boosted signal is substantially the same as the boosted signal.

18. (Original) The circuit of Claim 17, wherein the first boosted switch circuit, the second boosted switch circuit, the first dummy circuit, and the second dummy circuit are each substantially the same size.

19. (Original) The circuit of Claim 17, wherein the first boosted switch circuit is coupled between the second node and the first dummy circuit, the first dummy circuit is coupled between the first boosted switch circuit and the third node, the second dummy circuit is coupled between the second node and the second boosted circuit, and wherein the second boosted switch circuit is coupled between the second dummy circuit and the third node.

20. (Original) A circuit for sampling and holding, comprising:

a means for coupling a first node to a second node during a sample phase;

a means for storing charge at the second node;

a means for providing a boosted signal from a clock signal such that the boosted signal substantially corresponds to a boosted voltage during the hold phase, and such that the boosted voltage exceeds a high power supply voltage, wherein the clock signal is configured to alternate between a first voltage level and a second voltage level, and wherein the second voltage level corresponds to the high power supply voltage; and

a means for coupling a second node to a third node during a hold phase, comprising:

a means for opening and closing a boosted switch circuit in response to the boosted signal; and

a means for absorbing channel charge from the boosted switch circuit if the boosted switch circuit closes, wherein the means for absorbing the channel charge is responsive to another boosted signal.

21. (New) A circuit for sampling and holding, comprising:

a processing circuit that is operable to provide a digital output signal, wherein the processing circuit is time-interleaved such that the processing circuit includes a first processing channel that is

operable to provide the digital output signal at a first time and a second processing channel that is operable to provide the digital output signal at a second time; and

a sample-and-hold circuit that is interleaved by at least two such that a speed of the sample-and-hold circuit is approximately at least doubled without substantially decreasing the processing time allowed for the processing circuit.

22. (New) A circuit for sampling and holding, comprising:

a processing circuit that is interleaved such that the processing circuit includes a first processing channel and a second processing channel;

a first sample-and-hold channel that is coupled to the first processing channel;

a boost circuit that is coupled to the first sample-and-hold channel, wherein the boost circuit is capable of providing a boosted voltage that exceeds a power supply voltage; and

a second sample-and-hold channel that is coupled to the second processing channel.